**Amendments to the Specification:**

Page 5, line 9, to page 6, line 11:

In other words, the invention achieves the above objects with a semiconductor module with a plurality of interface circuits has a configuration for the self-test of interface circuits, which comprises:

- two equally sized groups of interface circuits such that each interface circuit of the first group is assigned exactly one interface circuit of the second group,
- a circuit which interacts with the first group and serves for generating test signals which can be output via the interface circuit of the first group;
- a circuit which interacts with the second group and serves for receiving and processing test signals received via the interface circuits of the second group, so that a connection of the assigned interface circuits of the first and second groups enables a ~~self-test~~ self-test,
- the first and second groups of interface circuits having a separate voltage supply.

The invention is thus based on the concept of utilizing the interface circuits for testing themselves. To that end, the interface circuits are divided into two groups and test signals are output via the first group of interface circuits.

Via an external connection of the first group to the second group of interface circuits, during the ~~self-test~~ self-test, the test signals pass to the second group of interface circuits, where the test signals are received and processed in a circuit.

Page 8, line 14, to page 9, line 2:
Furthermore, a low-frequency signal voltage can be modulated onto at least one of the supply voltages of the interface groups. Preferably, ~~low-frequency~~ low-frequency sinusoidal signals of different frequency are modulated onto both supply voltages, thereby achieving a timing test which is very close to the application and even goes beyond the possibilities of an external test system.

Overall, the invention described permits a relatively short test time without necessitating ~~high-precision~~ high-precision test systems with regard to the timing control or voltage. The customary mismatch when the ~~high-speed~~ high-speed pins are capacitively coupled to the test system is obviated. Moreover, only a small additional hardware outlay arises on the semiconductor module, since no PLL or DLL logic is required.

Page 11, lines 16-19:

In the housed state, the semiconductor module 10 is situated in a package 40. The terminals of the interface circuits are routed out at pins ~~42 - - - 49~~ 42 - 49 of the package. The supply voltage 38, 39 for the logic core 36 is additionally provided.

Page 12, lines 4-11:

During test operation, first of all the LFSR 34a, 34b generates a series of test signals which are output via the interface circuits 14a, 14b and pass via the connections 52, 54 to the interface circuits 12a, 12b and from there to the MISR 30, which calculates a signature from the test signals. After a specific number of received test signals, the calculated signature is compared with a prescribed signature for ~~fault- free~~ fault-free functioning of the interface circuit.

Page 14, lines 11, to page 15, line 3:

The connections can again be influenced capacitively, inductively or resistively via switches 156. In addition, Fig. 2 shows the possibility of modulating different ~~low- frequency~~ low-frequency sinusoidal signals U1 and U2, respectively, on the two supply voltages. During the fast self-test, the fast frequency is provided by the PLL of the module 100 itself. Comprehensive test coverage is achieved by virtue of the

modulated supply voltage fluctuations U1, U2 in combination with the PLL jitter that is really present. In this case, the LFSR/MISR circuit is situated upstream of the multiplexer circuit in the slow frequency range and is simple to realize.

With reference to Fig. 3, after the separation and packaging the two supply voltage pads 128, 129 in the package 140 are externally accessible only through a single pin 148, so that it is then not possible to effect the self-test with a separated supply voltage. However, a ~~self- test~~ self-test is possible here, too, with a DUT board 250, similarly to the process described above in connection with Fig. 1.